IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-6. (Canceled)

7. (Currently Amended) ~~The~~ A semiconductor integrated circuit ~~of claim 6, wherein each of the stage elements further comprises~~ comprising:

a system bus divided into stages and configured to transfer signals;

stage elements configured to connect the stages in series and operate in a divided mode transferring signals from a stage on an input side to a stage on an output side in synchronization with a clock signal and in a through mode that always passes signals from the stage on the input side to the stage on the output side; and

a plurality of function modules connected to the different stages,

wherein each of the stage elements comprises:

a storage circuit configured to hold a signal transferred from the stage on the input side, comprising a flip-flop circuit configured to latch and hold the signal in synchronization with the clock signal; and

a selector comprising:

a first input terminal connected to the stage on the input side;

a second input terminal connected to the stage on the input side through the flip-flop circuit;

an output terminal connected to the stage on the output side; and

a switching terminal configured to receive a through signal switching connections between the first and second input terminals and the output terminal from one to another, wherein:

the selector connects the second input terminal to the output terminal in the divided mode and connects the first input terminal to the output terminal in the through mode.

8. (Currently Amended) ~~The~~ A semiconductor integrated circuit ~~of claim 6, wherein the stage element comprises~~ comprising:

a system bus divided into stages and configured to transfer signals;

stage elements configured to connect the stages in series and operate in a divided mode transferring signals from a stage on an input side to a stage on an output side in synchronization with a clock signal and in a through mode that always passes signals from the stage on the input side to the stage on the output side; and

a plurality of function modules connected to the different stages,

wherein each of the stage elements comprises:

a storage circuit configured to hold a signal transferred from the stage on the input side, comprising a flip-flop circuit configured to latch and hold the signal in synchronization with the clock signal; and

a pulse generator configured to generate pulse signals synchronous to the clock signal in the divided mode, and in the through mode, stop the generation of the pulse signals and keep the storage circuit passing the signal therethrough, and the flip-flop circuit latches and holds the signal in synchronization with the pulse signals.

9. (Canceled)

10. (Currently Amended) ~~The~~ A semiconductor integrated circuit ~~of claim 1,~~ comprising:

a system bus divided into stages and configured to transfer signals;

stage elements configured to connect the stages in series and operate in a divided mode transferring signals from a stage on an input side to a stage on an output side in synchronization with a clock signal and in a through mode that always passes signals from the stage on the input side to the stage on the output side; and

a plurality of function modules connected to the different stages,

wherein the plurality of function modules operate in synchronization with the clock signal.

11. (Currently Amended) ~~The~~ A semiconductor integrated circuit ~~of claim 9,~~ comprising:

a system bus divided into stages and configured to transfer signals;

stage elements configured to connect the stages in series and operate in a divided mode transferring signals from a stage on an input side to a stage on an output side in synchronization with a clock signal and in a through mode that always passes signals from the stage on the input side to the stage on the output side; and

a plurality of function modules connected to the different stages,

wherein each of the stage elements comprises:

a storage circuit configured to hold a signal transferred from the stage on the input side, comprising a flip-flop circuit configured to latch and hold the signal in synchronization with the clock signal; and

a clock controller configured to supply clock signals to the flip-flop circuit in the divided mode, and in the through mode, stop the supply of the clock signals to the flip-flop circuit and keep the storage circuit passing the signal therethrough,

wherein the supply of the clock signals to the function modules stops in the through mode.

12. (New) The semiconductor integrated circuit of claim 10, further comprising a clock transfer circuit configured to supply the clock signal to the stage elements in the divided mode and stop the supply of the clock signal to the stage elements in the through mode.

13. (New) The semiconductor integrated circuit of claim 10, wherein the function modules have equivalent functions.

14. (New) The semiconductor integrated circuit of claim 13, wherein the function modules each comprise a memory having a function of storing data.

15. (New) The semiconductor integrated circuit of claim 10, wherein each of the stage elements comprises a storage circuit configured to hold a signal transferred from the stage on the input side.

16. (New) The semiconductor integrated circuit of claim 15, wherein the storage circuit comprises a flip-flop circuit configured to latch and hold the signal in synchronization with the clock signal.

17. (New) The semiconductor integrated circuit of claim 16, wherein the stage element comprises a clock controller configured to supply clock signals to the flip-flop circuit in the divided mode, and in the through mode, stop the supply of the clock signals to the flip-flop circuit and keep the storage circuit passing the signal therethrough.